IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Original): A phase-change memory device comprising:

a substrate;

a plurality of first parallel wiring lines formed above said substrate;

a plurality of second parallel wiring lines formed above said substrate to cross the first wiring lines while being electrically insulated therefrom; and

a plurality of memory cells disposed at respective crossing points of said first wiring lines and said second wiring lines, each said memory cell having one end connected to said first wiring line and the other end connected to said second wiring line, wherein

said memory cell comprises:

a variable resistive element for storing as information a resistance value determined due to phase change between crystalline and amorphous states thereof; and

a Schottky diode connected in series to said variable resistive element.

Claim 2 (Original): The phase-change memory device according to claim 1, wherein

said Schottky diode is series-connected to said variable resistive element while having its polarity with said first wiring line side as an anode and with said second wiring line side as a cathode;

said first wiring lines and second wiring lines are potentially fixed in a way such that said Schottky diode of each said memory cell becomes reverse-biased when nonselected; and

said first wiring lines and second wiring lines are selectively pulse-driven during data reading or writing to cause said Schottky diode of said memory cell selected by these lines to become forward-biased.

Claim 3 (Original): A phase-change memory device comprising:

a semiconductor substrate;

a plurality of semiconductor layers formed in said semiconductor substrate so that these are arrayed in a matrix form while being partitioned by an element isolation dielectric film;

diodes each formed at its corresponding semiconductor layer with a metal electrode as a terminal electrode, the metal electrode being formed at part of a surface of each said semiconductor layer;

a plurality of first wiring lines provided to commonly connect said diodes as arrayed in one direction of the matrix;

an interlayer dielectric film covering said first wiring lines;

metal plugs buried in space portions of said first wiring lines of said interlayer dielectric film and being in ohmic contact with each said semiconductor layer;

a chalcogenide layer being formed above said interlayer dielectric film and having its bottom surface in contact with said metal plugs; and

a plurality of second wiring lines provided to cross said first wiring lines while being in contact with an upper surface of said chalcogenide layer.

Claim 4 (Original): The phase-change memory device according to claim 3, wherein each said diode is a Schottky diode with said metal electrode as an anode electrode.

Claim 5 (Original): The phase-change memory device according to claim 3, wherein said semiconductor layers are disposed at a pitch of 2F in the direction of said first wiring lines and also disposed at a pitch of 3F in the direction of said second wiring lines, where F is a minimal device-feature size; and

said first wiring lines and said metal plugs are alternately formed at a pitch of 3F in said second wiring line direction in such a way as to be connected to both end portions of each said semiconductor layer in said second wiring line direction.

Claim 6 (Original): A phase-change memory device comprising:

an insulative substrate;

a plurality of first wiring lines formed in parallel with each other above said insulative substrate;

memory cells being formed over each said first wiring line so that one end is connected to each said first wiring line, each said memory cell having a stacked structure of a variable resistive element and a diode, said variable resistive element storing as information a resistance value determined due to phase change between crystalline and amorphous states thereof; and

a plurality of second wiring lines formed over said memory cells to commonly connect together the other end portions of said memory cells arrayed in a direction crossing said first wiring lines.

Claim 7 (Original): The phase-change memory device according to claim 6, wherein each said memory cell comprises:

a diode buried in an interlayer dielectric film formed above said first wiring liners so that an upper terminal surface becomes substantially the same in plane position as said interlayer dielectric film while letting a lower terminal surface be connected to a corresponding one of said first wiring lines; and

a chalcogenide layer formed above said interlayer dielectric film with said diode buried therein so that its bottom surface is connected to said upper terminal surface of said diode, said chalcogenide layer becoming said variable resistive element.

Claim 8 (Original): The phase-change memory device according to claim 6, wherein said diode is a Schottky diode with said first wiring line side as an anode terminal.

Claim 9 (Original): A phase-change memory device comprising:

an insulative substrate; and

a plurality of memory cell arrays stacked over said insulative substrate, wherein each said memory cell array comprises:

a plurality of first wiring lines extending in parallel with each other;

a plurality of memory cells being formed above each said first wiring line in such a manner that one end is connected to each said first wiring line and each comprising a stacked structure of a variable resistive element and a diode, said variable resistive element storing as information a resistance value determined due to phase change between crystalline! and amorphous states thereof; and

a plurality of second wiring lines formed above said memory cells to commonly connect the other ends of said memory cells arrayed in a direction crossing said first wiring lines.

Claim 10 (Original): The phase-change memory device according to claim 9, wherein at least one of said first wiring lines and second wiring lines is shared by two cell arrays adjacent in an up-down direction.

Claim 11 (Original): The phase-change memory device according to claim 9, wherein

a layer stack order of said variable resistive element and diode is identical between adjacent cell arrays in an up-down direction.

Claim 12 (Original): The phase-change memory device according to claim 9, wherein

a layer stack order of said variable resistive element and diode is inverse between adjacent cell arrays in an up-down direction.

Claim 13 (Previously Presented): The phase-change memory device according to claim 6, wherein

said first and second wiring lines are formed with a line/space of 1F/1F, where F is a minimum feature size; and

said memory cells are buried in respective crossing points of said first and second wiring lines.

Claim 14 (Original): The phase-change memory device according to claim 9, wherein

said diode of each said memory cell is a Schottky diode being series-connected to said variable resistive element and while having its polarity with said first wiring line side as an anode and with said second wiring line side as a cathode;

said first wiring lines and said second wiring lines are potentially fixed in such a way that said diode of each said memory cell becomes reverse-biased when nonselected; and

during data read or write, said first wiring lines and second wiring lines are selectively pulse-driven to cause said diode of said memory cell selected by these lines to become forward-biased.

Claim 15 (Currently Amended): [[The]] A phase-change memory ~~according to any one of claims 1, 3, 6 and 9, further~~ comprising:

a substrate;

a plurality of first parallel wiring lines formed above said substrate;

a plurality of second parallel wiring lines formed above said substrate to cross the first wiring lines while being electrically insulated therefrom;

a plurality of memory cells disposed at respective crossing points of said first wiring lines and said second wiring lines in such a manner that one ends thereof are connected to said first wiring lines and the other ends to said second wiring lines, said memory cell comprising a variable resistive element for storing a resistance value determined due to phase change between crystalline and amorphous states thereof, and a diode connected in series to said variable resistive element; and

selector circuits for fixing said first wiring lines to a state lower in potential than said second wiring lines when nonselected and for selectively supplying positive and negative logic pulses to said first and second wiring lines respectively during data reading or writing.

Claim 16 (Original): The phase-change memory device according to claim 15, wherein

each said selector circuit comprises:

a first select transistor for transferring said positive logic pulse to said first wiring line;

a second select transistor for transferring said negative logic pulse to said second wiring line;

a first reset-use transistor for holding said first wiring line at a first potential level when nonselected; and

a second reset-use transistor for holding said second wiring line at a second potential level higher than the first potential level when nonselected.

Claim 17 (Original): The phase-change memory device according to claim 15, further comprising a sense amplifier circuit for comparing a current of said memory cell selected by said selector circuits to a reference value to thereby detect data.

Claim 18 (Original): The phase-change memory device according to claim 17, wherein

said sense amplifier circuit comprises at least one of:

a first current detection circuit for comparing to a reference value a current flowing in said first wiring line when said positive and negative logic pulses are given to said first and second wiring lines respectively and for performing level determination; and

a second current detection circuit for comparing to a reference value a current flowing in said second wiring line when said positive and negative logic pulses are given to said first and second wiring lines respectively and for performing level determination.

Claim 19 (Original): The phase-change memory device according to claim 17, wherein

said sense amplifier circuit comprises:

a dummy cell having its resistance value midway between a high resistance state and a low resistance state of said memory cells;

a first resistor interposed between said first wiring line and a first power supply line to which said positive logic pulse is given;

a second resistor interposed between said second wiring line and a second power supply line to which said negative logic pulse is given;

a third resistor interposed between one end of said dummy cell and said first power supply line;

a fourth resistor interposed between the other end of said dummy cell and said second power supply line;

a first operational amplifier for comparison between an intermediate tap output voltage of said first resistor and a voltage at a connection node of said third resistor and said dummy cell; and

a second operational amplifier for comparison between an intermediate tap output voltage of said second resistor and a voltage at a connection node of said fourth resistor and said dummy cell.

Claim 20 (Currently Amended): [[The]] A phase-change memory device ~~according to claim 9, wherein~~ comprising an insulative substrate and a plurality of memory cell arrays stacked over said insulative substrate, wherein

each said memory cell array comprises:

a plurality of first wiring lines extending in parallel with each other;

a plurality of memory cells formed above said first wiring line in such a manner that one ends are connected to said first wiring lines, each said memory cell comprising a stacked structure of a variable resistive element and a diode, said variable resistive element storing as information a resistance value determined due to phase change between crystalline and amorphous states thereof; and

a plurality of second wiring lines formed above said memory cells to commonly connect the other ends of said memory cells arrayed in a direction crossing said first wiring lines, and wherein

write and read of multiple-value information are performed by combination of a high resistance state and a low resistance state of the respective memory cells accessed simultaneously in said plurality of memory cell arrays.

Claim 21 (Original): The phase-change memory device according to claim 20, wherein

said plurality of cell arrays has a first cell array and a second cell array stacked over said first cell array, said first and second cell arrays sharing said first wiring lines; and

write and read of four-value information are performed by combination of said high resistance state and said low resistance state of two memory cells; accessed simultaneously in said first and second cell arrays.

Claim 22 (Original): The phase-change memory device according to claim 21, further comprising a sense amplifier circuit for detection of said four-value information, wherein

said sense amplifier circuit comprises:

a first current detection circuit for comparing a current flowing in said second wiring line of said first cell array to a reference value and for performing level determination;

a second current detection circuit for comparing a current flowing in said first wiring line shared by said first and second cell arrays to a reference value and for performing level determination; and

a third current detection circuit for comparing a current flowing in said second wiring line of said second cell array to a reference value and for performing level determination.

Claim 23 (Original): The phase-change memory device according to claim 20, wherein

said plurality of cell arrays has a first cell array, a second cell array stacked over said first cell array, said first and second cell arrays sharing said first wiring lines, and a third cell array stacked over said second cell array, said second and third cell arrays sharing said second wiring lines; and

write and read of eight-value information are performed by combination of said high resistance state and said low resistance state of three memory cells accessed simultaneously in said first to three cell arrays.

Claim 24 (Original): The phase-change memory device according to claim 23, further comprising a sense amplifier circuit for detection of said eight-value information, wherein

said sense amplifier circuit comprises:

a first current detection circuit for comparing a current flowing in said second wiring line of said first cell array to a reference value and for performing level determination;

a second current detection circuit for comparing a current flowing in said first wiring line shared by said first and second cell arrays to a reference value and for performing level determination;

a third current detection circuit for comparing a current flowing in said second wiring line shared by said second and third cell arrays to a reference value and for performing level determination; and

a fourth current detection circuit for comparing a current flowing in said first wiring line of said third cell array to a reference value and for performing level determination.

Claim 25 (Original): The phase-change memory device according to claim 24, wherein

said second current detection circuit comprises two current detection units for determining a difference in current value between a case of two selected memory cells of said first and second cell arrays being both in said low resistance state and a case of either one being in said low resistance state.

Claim 26 (Original): The phase-change memory device according to claim 24, wherein

said third current detection circuit comprises two current detection units for determining a difference in current value between a case of two selected memory cells of said second and third cell arrays being both in said low resistance state and a case of either one being in said low resistance state.

Claim 27 (Original): The phase-change memory device according to claim 15, further comprising a write circuit for supplying a positive logic pulse and a negative logic pulse to said first wiring line and said second wiring line respectively with respect to a memory cell as selected by said selection circuit, for writing said low resistance state due to complete overlap of pulse widths of said positive logic pulse and negative logic pulse, and for wiring said high resistance state due to partial overlap of pulse widths of said positive logic pulse and negative logic pulse.

Claim 28 (Original): The phase-change memory device according to claim 27, wherein

said write circuit has a pulse voltage booster circuit for selectively boosting either one of said positive logic pulse and said negative logic pulse at an overlap portion of pulse widths of said positive logic pulse and negative logic pulse when writing said high resistance state.

Claim 29 (Original): The phase-change memory device according to claim 20, further comprising a write circuit for writing, based on write pulse width control, multi-value information into a plurality of simultaneously accessed memory cells of said plurality of cell arrays, said multi-value information being represented by combination of said high resistance state and said low resistance state within said plurality of simultaneously accessed memory cells.

Claim 30 (Original): The phase-change memory device according to claim 29, wherein

said write circuit comprises:

a pulse generation circuit for generating two types of pulses different in pulse width from each other; and

a logic gate circuit for determining in accordance with said multi-value information the time width of a write pulse being given between the simultaneously selected first and second wiring lines of a cell array by selection and combination of two types of pulses as output from said pulse generation circuit.

Claim 31 (Original): The phase-change memory device according to claim 29, wherein

said write circuit comprises:

a pulse generation circuit for generating two types of pulses with a constant pulse width and with a time difference therebetween; and

a logic gate circuit for determining in accordance with said multi-value information the time width of an overlap of said positive logic pulse and said negative logic pulse being given to the simultaneously selected first and second wiring lines of a cell array respectively by selection and combination of said two types of pulses as output from said pulse generation circuit.

Claim 32 (Previously Presented): The phase-change memory device according to claim 30, wherein

said write circuit comprises a pulse voltage booster circuit for selectively boosting said positive logic pulse or said negative logic pulse being output from said logic gate circuit in accordance with said multi-value information to be written.

Claim 33 (Original): The phase-change memory device according to claim 9, wherein

in said plurality of cell arrays, a plurality of cell blocks are defined as three-dimensional cell assemblies, each cell blocks being surrounded by first virtual boundaries with a predetermined interval being in parallel to said first wiring lines and perpendicular to a cell array plane and second virtual boundaries with a prespecified interval being in parallel to said second wiring lines and perpendicular to said cell array plane; and

data access is performed in units of said cell blocks.

Claim 34 (New): A memory device comprising:

a semiconductor substrate;

a plurality of semiconductor regions formed on the semiconductor substrate to be separated from each other by an insulating film buried in the semiconductor substrate;

diodes formed on the semiconductor regions;

a plurality of first wiring lines formed on the substrate to couple the diodes arranged in one direction;

an interlayer dielectric film formed to cover the first wiring lines;

metal plugs buried in the interlayer dielectric film to be in contact with the semiconductor layers;

variable resistance elements formed on the metal plugs; and

a plurality of second wiring lines formed on the variable resistance elements to couple them arranged in the direction crossing the first wiring lines.

Claim 35 (New): The memory device according to claim 34, wherein

the diodes are Shottky diodes, in each of which the first wiring line serves as a metal anode, or a metal anode is formed independently of the first wiring line.

Claim 36 (New): The memory device according to claim 34, wherein

the diodes are p-n junction diodes.

Claim 37 (New): The memory device according to claim 34, wherein

the variable resistance elements are defined as areas sandwiched by the metal plugs and the second wiring lines in a variable resistance element film formed over the metal plugs and the interlayer dielectric film.

Claim 38 (New): The memory device according to claim 34, wherein

the variable resistance elements are patterned to be independent of each other and disposed on the metal plugs.

Claim 39 (New): The memory device according to claim 34, wherein

the semiconductor regions are arranged at a pitch of 2F in the direction of the first wiring line and at a pitch of 3F in the direction of the second wiring line, where F is a fixed value.

Claim 40 (New): A method for fabricating a memory device comprising:

burying an insulating film in a semiconductor substrate to partition it into a plurality of semiconductor regions;

forming diodes on the semiconductor regions;

forming a plurality of first wiring lines on the substrate to couple the diodes arranged in one direction;

forming an interlayer dielectric film to cover the first wiring lines;

burying metal plugs in the interlayer dielectric film to be in contact with the semiconductor regions;

forming variable resistance elements on the metal plugs to constitute memory cells together with the diodes; and

forming a plurality of second wiring lines on the variable resistance elements to couple them arranged in the direction crossing the first wiring lines.

Claim 41 (New): The method according to claim 40, wherein

the diodes are formed as Shottky diodes, in each of which the first wiring line serves as a metal anode, or a metal anode is formed independently of the first wiring line.

Claim 42 (New): The method according to claim 40, wherein

the diodes are formed as p-n junction diodes.

Claim 43 (New): The method according to claim 40, wherein

the variable resistance elements are defined as areas sandwiched by the metal plugs and the second wiring lines in a variable resistance element film formed over the metal plugs and the interlayer dielectric film.

Claim 44 (New): The method according to claim 40, wherein

the variable resistance elements are patterned to be independent of each other and disposed on the metal plugs.

Claim 45 (New): The method according to claim 40, wherein

the semiconductor regions are! arranged at a pitch of 2F in the direction of the first wiring line and at a pitch of 3F in the direction of the second wiring line, where F is fixed value.

Claim 46 (New): A memory device comprising;

a substrate;

a plurality of first wiring lines formed above the substrate;

a first interlayer dielectric film formed between the first wiring lines;

memory cells formed on the first wiring lines, each said memory cell having a stacked structure of a variable resistance element and a diode;

a second interlayer dielectric film formed around the memory cells; and

a plurality of second wiring lines formed over the memory cells and the second interlayer dielectric film to cross the first wiring lines and couple the memory cells arranged in the direction the second wiring lines.

Claim 47 (New): The memory device according to claim 46, wherein

the diode is a Shottky diode, in which the first wiring line serves as a metal anode.

Claim 48 (New): The memory device according to claim 46, wherein

the substrate is a semiconductor substrate on which an insulating film is formed.

Claim 49 (New): The memory device according to claim 46, wherein

the first wiring lines and the second wiring lines are arranged with a line/space of 1F/1F, where F is a fixed value.

Claim 50 (New): A method for fabricating a memory device comprising:

forming a plurality of first wiring lines above a substrate;

forming a first interlayer dielectric film between the first wiring lines;

forming memory cells on the first wiring lines, the memory cell having a stacked structure of a variable resistance element and a diode;

forming a second interlayer dielectric film around the memory cells; and

forming a plurality of second wiring lines over the memory cells and the second interlayer dielectric film to cross the first wiring lines and couple the memory cells arranged in the direction the second wiring lines.

Claim 51 (New): The method according to claim 50, wherein

the procedure of forming the memory cells comprises:

depositing a semiconductor layer over the first wiring lines and the first interlayer dielectric film;

depositing a variable resistance element layer on the semiconductor layer; and

patterning the variable resistance element layer and the semiconductor layer to form the respective memory cells disposed on the first wiring lines, the diode of each memory cell being formed as an Shottky diode, in which the first wiring line serves as a metal anode.

Claim 52 (New): The method according to claim 50, wherein

the first wiring lines and the second wiring lines are arranged with a line/space of 1F/lF, where F is a fixed valve.

Claim 53 (New): A memory device comprising a substrate and a plurality of memory cell arrays stacked above the substrate, wherein

each said memory cell array comprises:

a plurality of first wiring lines formed on an insulative surface of an underlying substrate;

a first interlayer dielectric film buried between the first wiring lines;

memory cells formed on the first wiring lines, each said memory cell having a variable resistance element to be set at a resistance value;

a second interlayer dielectric film formed around the memory cells; and

a plurality of second wiring lines formed over the memory cells and the second interlayer dielectric film to couple the memory cells arranged in the direction of the second wiring lines.

Claim 54 (New): The memory device according to claim 53, wherein

each said memory cell has a stacked structure of the variable resistance element and a diode, and wherein

at least one of the first wiring lines and the second wiring lines are shared by adjacent two memory cell arrays, in which the diodes are arranged with reverse directions.

Claim 55 (New): The memory device according to claim 53, wherein

each said memory cell has a stacked structure of the variable resistance element and a diode, and wherein

adjacent two memory cell arrays have the same stack order of the variable resistance element and the diode.

Claim 56 (New): The memory device according to claim 53, wherein

each said memory cell has a stacked structure of the variable resistance element and a diode, and wherein

adjacent two memory cell arrays have the reverse stack order of the variable resistance element and the diode.

Claim 57 (New): A memory device comprising:

a substrate;

a plurality of memory cell arrays stacked above the substrate, each said memory cell array including first wiring lines and second wiring lines crossing each other, and memory cells disposed between the first wiring lines and the second wiring lines at crossing points

thereof, each said memory cell having a stacked structure of a variable resistance element and a diode; and

selector circuits formed on the substrate for fixing the first and second wiring lines in potential in such a manner as to reverse-bias the diodes in non-selected memory cells, and for driving a first wiring line and a second wiring line in a memory cell array in such a manner as to forward-bias the diode in a selected memory cell during data reading or writing.

Claim 58 (New): The memory device according to claim 57, wherein

the anode of the diode is coupled to the first wiring line, and wherein the selector circuit comprises:

a first select transistor for transferring a positive logic pulse to a first wiring line;

a second select transistor for transferring a negative logic pulse to a second wiring line;

a first reset transistor for setting a first wiring line at a first potential when non-selected; and

a second reset transistor for setting a second wiring line at a second potential when non-selected.

Claim 59 (New): A memory device comprising:

a substrate;

a memory cell array formed above the substrate to have first wiring lines and second wiring lines crossing each other, and memory cells disposed between the first wiring lines and the second wiring lines at crossing points thereof, each said memory cell having a stacked structure of a variable resistance element and a diode; and

a sense amplifier formed on the substrate, wherein

the sense amplifier comprises at least one of:

a first current detecting circuit for comparing a current flowing in a selected first wiring line with a reference current when a positive logic pulse and a negative logic pulse are applied to the selected first wiring line and a selected second wiring line, respectively, to forward-bias the diode in a selected memory cell; and

a second current detecting circuit for comparing a current flowing in a selected second wiring line with a reference current when a positive logic pulse and a negative logic pulse are applied to a selected first wiring line and the selected second wiring line, respectively, to forward-bias the diode in a selected memory cell.

Claim 60 (New): The memory device according to claim 59, wherein

the sense amplifier comprises:

a dummy cell having a resistance value set midway between a high resistance state and a low resistance state of the memory cell;

a first resistor interposed between a first wiring line and a first power supply line, to which the positive logic pulse is given;

a second resistor interposed between a second wiring line and a second power supply line, to which the negative logic pulse is given;

a third resistor interposed between one end of the dummy cell and the first power supply line;

a fourth resistor interposed between the other end of the dummy cell and the second power supply line;

a first operational amplifier for comparing an output voltage at an intermediate tap of the first resistor with a voltage at a connection node of the third resistor and the dummy cell; and

a second operational amplifier for comparing an output voltage at an intermediate tap of the second resistor with a voltage at a connection node of the fourth resistor and the dummy cell.

Claim 61 (New): A memory device comprising:

a substrate;

a plurality of memory cell arrays stacked above the substrate, each said memory cell array including memory cells arranged therein, the memory cell having a stacked structure of a variable resistance element and a diode; and

a sense amplifier configured to sense memory cell data, wherein

multi-value data is storable in the memory cells selected one by one from the respective memory cell arrays, the multi-value data being defined by a combination of resistance states in the respective memory cells.

Claim 62 (New): The memory device according to claim 61, wherein

the multi-value data is a four-value data defined by two bits storable in first and second memory cell arrays stacked.

Claim 63 (New): The memory device according to claim 62, wherein

each of the first and second memory cell arrays has first wiring lines and second wiring lines crossing each other, and the memory cells disposed between the first and second wiring lines at the crossing points thereof, the first and second memory cell arrays having stack orders reverse to each other and sharing the first wiring lines, and wherein

the sense amplifier comprises:

a first current detection circuit for comparing a current flowing in a second wiring line selected in the first memory cell array with a reference current;

a second current detection circuit for comparing a current flowing in a selected first wiring line shared by the first and second memory cell arrays with a reference current; and

a third current detection circuit for comparing a current flowing in a second wiring line selected in the second memory cell array with a reference current.

Claim 64 (New): The memory device according to claim 61, wherein

the multi-value data is an eight-value data defined by three bits storable in first, second and third memory cell arrays stacked.

Claim 65 (New): The memory device according to claim 64, wherein

each of the first, second and third memory cell arrays has first wiring lines and second wiring lines crossing each other and the memory cells buried between the first and second wiring lines at the crossing points thereof, the first and second memory cell arrays having stack orders reverse to each other and sharing the first wiring lines, the second and third memory cell arrays having stack orders reverse to each other and sharing the second wiring lines, and wherein

the sense amplifier comprises:

a first current detection circuit for comparing a current flowing in a second wiring line selected in the first memory cell array with a reference current;

a second current detection circuit for comparing a current flowing in a selected first wiring line shared by the first and second memory cell arrays with a reference current;

a third current detection circuit for comparing a current flowing in a selected second wiring line shared by the second and third memory cell arrays with a reference current; and

a fourth current detection circuit for comparing a current flowing in a first wiring line selected in the third memory cell array with a reference current.

Claim 66 (New): The memory device according to claim 65, wherein

at least one of the second and third current detection circuits has two operational amplifier systems with different reference values set for dissolving shrunk data.

Claim 67 (New): The memory device according to claim 61, wherein

the multi-value data is a sixteen-value data defined by four bits stored in first, second, third and fourth memory cell arrays stacked.

Claim 68 (New): The memory device according to claim 67, wherein each of the first, second, third and fourth memory cell arrays has first wiring lines and second wiring lines crossing each other, and the memory cells buried between the first and second wiring lines at the crossing points thereof, the first and second memory cell arrays having stack orders reverse to each other and sharing the first wiring lines, the second and third memory cell arrays having stack orders reverse to each other and sharing the second wiring lines, the third and fourth memory cell arrays having stack orders reverse to each other and sharing the first wiring lines, and wherein

the sense amplifier comprises:

a first current detection circuit for comparing a current flowing in a second wiring line selected in the first memory cell array with a reference current;

a second current detection circuit for comparing a current flowing in a selected first wiring line shared by the first and second memory cell arrays with a reference current, the

second current detection circuit having two operational amplifier systems with different reference values set for dissolving shrunk data;

a third current detection circuit for comparing a current flowing in a selected second wiring line shared by the second and third memory cell arrays with a reference current; and

a fourth current detection circuit for comparing a current flowing in a selected first wiring line shared by the third and fourth memory cell arrays with a reference current, the fourth current detection circuit having two operational amplifier systems with different reference values set for dissolving shrunk data; and

a fifth current detection circuit for comparing a current flowing in a second wiring line selected in the fourth memory cell arrays with a reference current.

Claim 69 (New): A memory device comprising:

a substrate;

a plurality of memory cell arrays stacked above the substrate, each said memory cell array including memory cells arranged therein, each said memory cell having a stacked structure of a variable resistance element and a diode; and

a write circuit configured to write a multi-value data defined by multiple bits storable one by one in the memory cells selected from the respective memory cell arrays.

Claim 70 (New): The memory device according to claim 69, wherein

the multi-value data is a four-value data defined by two bits stored in first and second memory cell arrays stacked, each of the first and second memory, cell arrays having first wiring lines and second wiring lines crossing each other, and the memory cells disposed between the first and second wiring lines at the crossing points thereof, the first and second

memory cell arrays having stack orders reverse to each other and sharing the first wiring lines, and wherein

the write circuit comprises:

a pulse generation circuit for generating two pulses, which are different in pulse width from each other; and

a logic circuit for generating negative logic write pulses and a positive logic write pulse by selection and combination of the two pulses to be given to the second wiring lines and the shared first wiring line simultaneously selected from the respective memory cell arrays, the overlap pulse width between the negative logic write pulse and the positive logic write pulse applied to a selected memory cell being defined in accordance with a to-be-written data bit.

Claim 71 (New): The memory device according to claim 70, wherein the write circuit further comprises a pulse voltage booster for boosting at least one of the negative and positive logic write pulses.

Claim 72 (New): The memory device according to claim 69, wherein

the multi-value data is a four-value data defined by two bits storable in first and second memory cell arrays stacked, each of the first and second memory cell arrays having first wiring lines and second wiring lines crossing each other, and the memory cells disposed between the first and second wiring lines at the crossing points thereof, the first and second memory cell arrays having stack orders reverse to each other and sharing the first wiring lines, and wherein

the write circuit comprises:

a pulse generation circuit for generating two pulses, one of which is delayed to the other for a certain time length; and a logic circuit for generating negative logic write pulses and a positive logic write pulse by selection and combination of the two pulses to be given to the second wiring lines and the shared first wiring line selected from the respective memory cell arrays, the overlap time width between the negative logic write pulse and the positive logic write pulse applied to a selected memory cell being defined in accordance with a to-be-written data bit.

Claim 73 (New): The memory device according to claim 72, wherein

the write circuit further comprises a pulse voltage booster for boosting at least one of the negative and positive logic write pulses.

Claim 74 (New): The memory device according to claim 69, wherein

the multi-value data is an eight-value data defined by three bits storable one by one in first, second and third memory cell arrays stacked, each of the first, second and third memory cell arrays having first wiring lines and second wiring lines crossing each other, and the memory cells buried between the first and second wiring lines at the crossing points thereof, the first and second memory cell arrays having stack orders reverse to each other and sharing the first wiring lines, the second and third memory cell arrays having stack orders reverse to each other and sharing the second wiring liners, and wherein

the write circuit comprises:

a pulse generation circuit for generating two pulses, one of which is delayed to the other for a certain time length; and

logic circuit for generating negative and positive logic write pulses by selection and combination of the two pulses to be given to the second and the first wiring lines selected

from the respective memory cell arrays, the overlap time width between the negative logic write pulse and the positive logic write pulse applied to a selected memory cell being defined in accordance to a to-be-written data bit.

Claim 75 (New): The memory device according to claim 74, wherein

the write circuit further comprises a pulse voltage booster for boosting at least one of the negative and positive logic write pulses.

Claim 76 (New): The memory device according to claim 69, wherein

the multi-value data is a sixteen-value data defined by four bits storable one by one in first, second, third, and fourth memory cell arrays stacked, each of the first, second, third and fourth memory cell arrays having first wiring lines and second wiring lines crossing each other, and the memory cells buried between the first and second wiring lines at the crossing points thereof, the first and second memory cell arrays having stack orders reverse to each other and sharing the first wiring lines, the second and third memory cell arrays having stack orders reverse to each other and sharing the second wiring lines, the third and fourth memory cell arrays having stack orders reverse to each other and sharing the first wiring lines, and wherein

the write circuit comprises:

a pulse generation circuit for generating two pulses, one of which is delayed to the other for a certain time length; and

logic circuit for generating negative and positive logic write pulses by selection and combination of the two pulses to be given to the second and the first wiring lines selected from the respective memory cell arrays, the overlap time width between the negative logic

write pulse and the positive logic write pulse applied to a selected memory cell being defined in accordance to a to-be-written data bit.

Claim 77 (New): The memory device according to claim 76, wherein

the write circuit further comprises a pulse voltage booster for boosting at least one of the negative and positive logic write pulses.

Claim 78 (New): A memory device comprising:

a substrate;

a plurality of memory cell arrays stacked above the substrate, each said memory cell array having bit lines coupled to one ends of memory cells and word lines coupled to the other ends, each said memory cell having a stacked structure of a variable resistance element and a diode, the memory cell arrays being partitioned in the bit line direction and in the word line direction into a plurality of cell blocks each serving as an access unit;

a bit line select circuit formed on the substrate to select one of the bit lines in one of the cell blocks; and

a word line select circuit formed on the substrate to select one of the word lines contained in of the cell blocks.

Claim 79 (New): The memory device according to claim 78, wherein

the bit line select circuit comprises:

a plurality of sets of bit line select lines disposed in correspondence to a plurality of layers of the bit lines, respectively, each set being shared by a plurality of the cell blocks arranged in the word line direction, on which bit line driving signals are supplied;

a plurality of sets of bit line selecting transistors arranged in correspondence to the plurality of sets of bit line select lines to couple the bit line select lines to the corresponding bit lines in the cell blocks; and

a decode gate circuit configured to select one of the cell blocks arranged in the word line direction and drive the bit line selecting transistors belonging to selected one of the cell blocks.

Claim 80 (New): The memory device according to claim 78, wherein

the word line select circuit comprises:

a plurality of sets of word line select lines disposed in correspondence to a plurality of layers of the word lines, each set being shared by a plurality of the cell blocks arranged in the bit line direction, on which word line driving signals are supplied;

a plurality of sets of word line selecting transistors arranged in correspondence to the plurality of sets of the word line select lines to couple the word line select lines to the corresponding word lines in the cell blocks; and

a decode gate circuit configured to select one of the cell blocks arranged in the bit line direction and drive the word line selecting transistors belonging to selected one of the cell blocks.

Claim 81 (New): The memory device according to claim 78, wherein

adjacent two memory cell arrays share the word lines disposed therein.

Claim 82 (New): The memory device according to claim 78, wherein

adjacent two memory cell arrays share the bit lines disposed therein.

Claim 83 (New): A memory device comprising:

a substrate; and

a plurality of memory cell arrays stacked above the substrate, each said memory cell array having bit lines coupled to one ends of memory cells and word lines coupled to the other ends, each said memory cell having a stacked structure of a variable resistance element and a diode, wherein

the memory cell arrays are partitioned in the bit line direction and in the word line direction into a plurality of cell blocks each with a three dimensional address space, and wherein

one of one-dimensional addresses defined in a two-dimensional address space of each said cell block with a three-dimensional address space is defined as a key address, in which a key string data is stored, and such a data search mode is adapted as to scan the one-dimensional addresses in the two-dimensional address space to detect the key string data, and then scan the remaining one-dimensional addresses to detect data belonging to the key string data.

Claim 84 (New): The memory device according to claim 83, further comprising:

a bit line select circuit formed on the substrate to select multiple bit lines in one of the cell blocks; and

a word line select circuit formed on the substrate to select multiple word lines in one of the cell blocks.

Claim 85 (New): The memory device according to claim 83, wherein

the key string data is defined by multiple bits simultaneously selected by multiple bit lines and a word line in a certain layer of one of the cell blocks.

Claim 86 (New): The memory device according to claim 83, wherein

the key string data is defined by multiple bits simultaneously selected by multiple word lines and a bit line in a certain layer of one of the cell blocks.

Claim 87 (New): The memory device according to claim 83, wherein

the key string data is defined by multiple bits simultaneously selected by multiple bit lines and multiple word lines arranged vertically in one of the cell blocks.

Claim 88 (New): The memory device according to claim 83, wherein

the device is used as a content reference memory.

Claim 89 (New): A memory device comprising:

a substrate; and

at least one memory cell array formed above the substrate to have bit lines coupled to one ends of memory cells and word lines coupled to the other ends, each said memory cell including a variable resistance element, wherein

one ends of a group of the memory cells are coupled in common to a word line via a selecting device while the other ends are coupled to different bit lines, respectively, in each said memory cell array.

Claim 90 (New): The memory device according to claim 89, wherein

the combination of data bits in the group serves as a multi-value data, and wherein

the multi-value data is written in such a manner that while the selecting device is on, bit line drive signals and a word line drive signal are applied to the bit lines and the word line,

respectively, with the respective overlap widths set between the bit line drive signals and the word line drive signal, the overlap widths being determined in accordance with the high resistance state and the low resistance state to be set in the memory cells in the group.

Claim 91 (New): The memory device according to claim 89, wherein

the selecting device is a transistor having source and drain regions formed on the substrate, the variable resistance elements in the group being formed to be in contact with the source region at one ends thereof while the other ends are coupled to different bit lines, respectively, formed above the variable resistance elements.

Claim 92 (New): The memory device according to claim 89, wherein

the selecting device is a diode formed on a word line formed, one end of the diode being in contact with the word line, the variable resistance elements in the group being formed to be in contact with one terminal of the diode at one ends thereof while the other ends are coupled to different bit lines, respectively, formed above the variable resistance elements.

Claim 93 (New): The memory device according to claim 89, wherein

a plurality of the memory cell arrays are so stacked as to share at least one of the bit lines and the word lines between adjacent two memory cell arrays.